Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application. In this listing, claim 1 is original and claims 2-16 have been added.

Listing of Claims:

1. (Original) A programmable logic device with high speed serial interface circuitry comprising:

programmable logic circuitry;

high speed serial interface circuitry, portions of which can selectively be coupled to portions of the programmable logic circuitry; and

a plurality of channels of functional sub-circuits for selectively coupling portions of the programmable logic circuitry and portions of the high speed serial interface circuitry.

2. (New) A programmable logic device comprising:

programmable logic circuitry;

serial interface circuitry for converting a serial data input signal to a plurality of parallel signals; and

pattern detection circuitry for detecting byte boundaries in the parallel signals.

3. (New) The device defined in claim 2 further comprising:

circuitry for applying to the programmable logic circuitry information from the parallel signals in accordance with the byte boundaries.

4. (New) The device defined in claim 3 wherein the circuitry for applying applies the information between two adjacent byte boundaries to the programmable logic circuitry in parallel.

5. (New) The device defined in claim 2 wherein the pattern detection circuitry is programmable with respect to what pattern is detected.

6. (New) The device defined in claim 2 wherein the pattern detection circuitry is responsive to the programmable logic circuitry with respect to what pattern is detected.

7. (New) The device defined in claim 2 further comprising:

circuitry for selectively applying information from the parallel signals to the programmable logic circuitry without regard for the byte boundaries.

8. (New) The device defined in claim 7 wherein the circuitry for selectively applying applies the information to the programmable logic circuitry in parallel.

9. (New) A programmable logic device comprising:

programmable logic circuitry; and

a plurality of serial interface circuits, each of which receives a respective one of a plurality of serial data input signals, and a first of the serial interface circuits including channel alignment circuitry for synchronizing data in that serial interface circuit with data in a second of the serial interface circuits.

10. (New) The device defined in claim 9 further comprising:

circuitry for applying to the programmable logic circuitry synchronized data from the first and second serial interface circuits.

11. (New) The device defined in claim 9 wherein the first serial interface circuit includes:

deserializer circuitry for converting the serial data input signal received by that serial interface circuit to a

plurality of parallel signals on which the channel alignment circuitry operates.

12. (New) The device defined in claim 9 wherein the first serial interface circuit further comprises:

circuitry for selectively applying data in the first serial interface circuit to the programmable logic circuitry without regard for synchronism with data in the second serial interface circuit.

13. (New) A programmable logic device comprising:

programmable logic circuitry;

serial interface circuitry for converting a serial data input signal to a plurality of parallel signals; and

ten bit to eight bit decoder circuitry for converting information from ten of the parallel signals to eight further parallel signals.

14. (New) The device defined in claim 13 further comprising:

circuitry for applying to the programmable logic circuitry information from the eight further parallel signals.

15. (New) The device defined in claim 13 further comprising:

circuitry for selectively applying information from the parallel signals to the programmable logic circuitry without regard for operation of the ten bit to eight bit decoder circuitry.

16. (New) A programmable logic device comprising:

programmable logic circuitry;

serial interface circuitry for converting a serial data input signal to a plurality of parallel signals, concurrent values of which in successive input character clock intervals represent successive input characters; and

rate matching circuitry for accommodating a possible difference between an input character clock rate and a programmable logic circuitry character clock rate by selectively deleting or inserting input characters.